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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,426	10/27/2003	Fei-Gwo Tsai	252016-2470	3358

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EXAMINER	
ROSASCO, STEPHEN D	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,426	TSAI ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Applicant's election without traverse of Group I claims 1-13, in the reply filed on 6/21/05, is acknowledged.

The disclosure is objected to because of the following informalities: there are numerous spelling and grammatical errors present, e.g., page 1, second paragraph, "this layers"; page 2, line 4, "The in this manner"; page 7, line 3, "useless surface are"; claim 1, second to last line, "B is applied to" the next line reads "is applied for" this is unclear.

Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mui et al. (2004/0038139) in view of Ki (6,475,684).

The claimed invention is directed to a method of creating a pattern in a layer of opaque material of a photolithographic exposure mask, comprising: defining an etch recipe for etching a product pattern A in an opaque material over a substrate of a photolithographic exposure mask that optimally meets Critical Diameter (CD) requirements of the product pattern, said etching a product pattern comprising a photoresist exposure mask; calculating the product pattern total Cr etch loading on the exposure mask; defining a residual or useless surface area of the exposure mask; if the

defined, optimum etch recipe meets the optimal Critical Diameter (CD) requirements, the exposure of the opaque material of the exposure mask is performed; if the defined, optimum etch recipe does not meet the optimal Critical Diameter (CD) requirements, then the Cr etch loading is modified by adding dummy patterns in unused areas of the photoresist exposure mask; if the addition of dummy patterns to the product pattern does not meet the Cr etch loading, then the Cr loading pattern A is separated into two parts B and C, such that pattern B meets Cr loading requirements, after which pattern B is applied to a first exposure process and pattern C is applied for a second exposure process.

The applicant discusses the limitations of the prior art in that it is clear that the longer the etch is applied the more of the exposed underlying material will be removed. It is thereby well known in the art that the etch removal rate of the underlying material depends on the pattern density of the material that needs to be removed, whereby smaller pattern features require a larger etch time for removal of the etched layer than larger pattern features etched in the underlying layer. This latter effect is known in the art as the loading effect, whereby it is clear that this loading effect can lead to serious problems of uneven etch removal rates over the surfaces of a substrate.

Mui et al. teach a method and apparatus for processing a semiconductor wafer is provided for reducing CD microloading variation. OCD metrology is used to inspect a wafer to determine pre-etch CD microloading, by measuring the CD of dense and isolated photoresist lines. Other parameters can also be measured or otherwise determined, such as sidewall profile, photoresist layer thickness, underlying layer thickness, photoresist pattern density, open area, etc. The inspection results are fed forward to the etcher to determine process parameters, such as resist trim time and/or etch conditions, thereby achieving the

desired post-etch CD microloading. In certain embodiments, the CD and profile measurements, trim, etch processing and post-etch cleaning are performed at a single module in a controlled environment.

And comprising: (a) measuring a D of an isolated pattern of a patterned layer formed on an underlying layer on the wafer; (b) measuring a CD of a dense pattern that is one of a plurality of patterns of the patterned layer disposed proximal to each other; (c) selecting a first set of process parameter values for a first process to be performed on the wafer, based on the measurements of the isolated pattern CD and the dense pattern CD; and (d) performing the first process on the wafer at a processing tool using the first set of process parameter values, comprising optically measuring the CDs of the isolated and dense patterns.

And wherein the first process is an etch process for forming a structure in the underlying layer.

The teachings of Mui et al. differ from those of the applicant in that the applicant teaches testing the etching on an unused part of the substrate to determine an etch recipe.

Ki teaches a method of correcting for variation in line width due to a loading effect generated when the material layer on a photomask substrate is dry-etched to have a desired pattern, the method comprising: obtaining a loading effect range delta by dividing the substrate into meshes, and supposing the distribution of a loading effect frequency f.sub.L representing the degree of a loading effect at an arbitrary mesh on the substrate from each of other meshes to be a Gaussian distribution.

And wherein the step of obtaining a loading effect range comprises: forming test patterns by exposing, developing and etching a photomask substrate, and measuring the

line width of the test pattern; dividing the test patterns by meshes, and calculating the loading density of test patterns which is defined as a ratio of an area to be etched to the area of each mesh; and calculating the loading effect of the test pattern at each mesh from an arbitrary loading effect range value according to the relationship EQU9 comparing the loading effects with the line widths of the test pattern at the meshes, and selecting a loading effect range in which the deviation between them is minimum; wherein x,y denotes the coordinate of the arbitrary mesh, and D(i,j) denotes the loading density of the test patterns in a mesh having a coordinate (i,j).

It would have been obvious to one having ordinary skill in the art to take the teachings of Mui et al. and combine them with the teachings of Ki in order to make the claimed invention because it is well known to test a chemical process in as close as possible to the actual conditions.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
07/20/05